AMENDMENTS TO THE SPECIFICATION

Please amend paragraph 24 as follows:

With reference to the accompanying drawings, FIG. 1 shows a starting point for the processing of the invention. In FIG. 1, a ~~silicon~~shallow-trench isolation (STI) 10 is provided of silicon dioxide (SiO_2)(hereinafter "oxide") having an active silicon (Si) region 12 in a portion thereof. A low temperature epitaxial (LTE) growth of silicon over this structure results in an intrinsic base layer 14 including a polysilicon portion 16 formed over STI 10 and a silicon intrinsic base portion 18 formed over active silicon region 12. Intrinsic base portion 18, as will become apparent below, provides an intrinsic base of a resulting self-aligned bipolar transistor structure 200 (FIG. 10).

Please amend paragraph 27 as follows:

FIG. 3 illustrates providing an emitter opening 50 using an emitter window mask layer 40 including an emitter window 42. Mask layer 40 may be any now known or later developed mask. At this point, as shown in FIG. 4, portions of extrinsic base layer 30 and second insulator layer ~~32~~34 are removed using an etch 46. Etch 46 extends through second insulator layer ~~32~~34 and extrinsic base layer 30 to expose a portion of the first insulator layer, i.e., landing pad 22. Etch 46 may be, for example, a selective reactive ion etch (RIE).

Please amend paragraph 30 as follows:

Next, as shown in FIG. 8, an oxidation 90 is conducted such as high pressure oxidation (HIPOX) 90 into emitter opening 50 to form an oxide portion 92 from conductor 80 (FIG. 7) within emitter opening 50 and from any conductor (not shown) formed on spacer 62 sidewalls and second insulator layer 34. Where a conductor is formed on spacer 62 sidewalls and second

insulator layer 34, oxidation 90 may form a continuous layer, which is later removed as will be discussed below. The amount of oxidation determines how far into conductor 80 the oxide portion 92 is formed, and as will be more apparent below, the spacing between extrinsic base layer 30 and emitter 110 (FIG. 10). As illustrated in FIG. 8, oxide portion 92 separates base link ~~82~~94 from emitter opening 50. In one embodiment, oxide portion 92 exists within emitter opening 50 and under at least a portion of spacer 62. Depending on the amount of oxidation provided, oxide portion 92 may also extend under a portion of extrinsic base layer 30. However, it is preferable, that oxide portion 92 be present only under spacer 62 to reduce the link resistance between extrinsic base layer 30 and intrinsic base layer 14, 18.

Please amend paragraphs 32-33 as follows:

As shown in FIG. 9, as a result of the above-described etch, oxide portion 92 is removed within emitter opening 50. Note, however, a remaining portion 102 of oxide portion 92 remains below at least a portion of spacer 62 and, possibly, a portion of extrinsic base layer 30 depending on the amount of oxidation. Remaining portion 102 provides insulation between extrinsic base layer 30 and a to-be-formed emitter. In addition, the size of remaining portion 102 defines a spacing between emitter 110 (FIG. 10) formed in the emitter opening ~~50~~ and base link 82 and/or extrinsic base layer 30.

Finally, as shown in FIG. 10, a polysilicon layer is deposited, patterned and etched to form emitter 110 within the emitter opening ~~50~~. It should be recognized that as a polysilicon layer is deposited, it may be re-aligned, i.e., some portion is converted to a monocrystalline silicon. Other processing to finalize transistor 200 may be conducted according to any now known or later developed manner. Transistor 200 includes an intrinsic base layer 14, 18; a raised

extrinsic base layer 30 in direct contact with intrinsic base layer 14, 18; an emitter 110 separated from raised extrinsic base layer 30 by spacer 62 and oxide section 102 (of converted conductor) under spacer 62; and a conductive base link 94 between oxide section 102 and raised extrinsic base layer 30. In addition, raised extrinsic base layer 30 is non-planar.